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A high stable on-chip CMOS temperature sensor

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Abstract: *A high stable CMOS temperature sensor is presented. A low-pass filter circuit is added in the output of traditional CMOS temperature sensor to improve the stability of its output,. The supply power voltage of the temperature sensor is 1.8V. The PSRR of the temperature sensor is -82dB in low frequency state. And the PSRR is -45dB in worst case. The OP-AMP of sensor has 63º phase margin. The output mode is voltage, whose linearity error is less than 0.2% and resolution ratio is more than 2.6mV/℃*

Keywords: *CMOS, temperature sensor, high stable, high precision, cascode*

I. Introduction

CMOS temperature sensor which is used in many kinds of control chips has so many advantages, such as small volume, low cost and low-power dissipation[1]. There are two kinds of CMOS temperature sensor structures. One use the sub-threshold MOSFET to sense temperature and the other use parasitic bipolar transistor to sense the temperature[2]. The former structure is not stable and work well as the temperature sensor of integrated chip. By comparison, the latter one is more stable and the reason is that all of the MOSFETs and parasitic bipolar transistors are working in saturation region. The circuit structure view of the later mentioned above is shown in fig. 1. The output mode is voltage and the working principle is as follows: Assuming that the breadth length ratio of MOSFET that M1 and M2 are equal, which means the current I_1 and I_2 are also equal. Meanwhile, the base-emitter voltage of Q1 (V_{be1}) and Q2 (V_{be2}) are constant. When the current I_2 increases, the positive electrode voltage (V_+) of operational amplifier (OP-AMP) also increases. The consequence is that the output of OP-AMP increases, and then the current I_2 decreases. During the whole process, the negative electrode voltage (V_-) of OP-AMP remain unchanged. So the OP-AMP is working in negative feedback mode and the two input voltage of OP-AMP are equal, which means $V_+ = V_-$. The relationship among V_{be1}, V_{be2}, $I2$ and R_1 can be work out, as shown in equation 1.

$$V_{be1} = I_2 R_1 + V_{be2} \quad (1)$$

So, I_2 can be expressed, as shown in equation 2.

$$I_2 = (V_{be2} - V_{be1})/R_1 \quad (2)$$

I_2 is a value which proportional to temperature, because V_{be1} and V_{be2} are almost proportional to temperature and R_1 is independent of temperature. M2 and M3 constitute a current mirror structure. Assuming that the breadth length ratio of MOSFET that M1 and M2 is n and R_2 is independent of temperature, the value of I_{PTAT} is n times of I_2. So I_{PTAT} is proportional to temperature. In fact, the temperature coefficient of R_1 and R_2 can cancel each other[3].

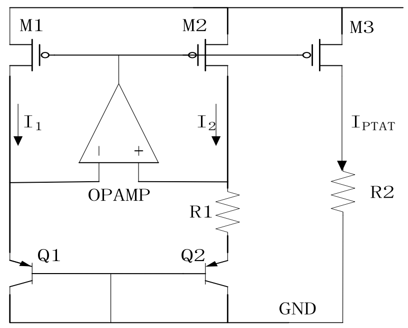

Fig.1 the basic circuit structure of CMOS temperature sensor

Recently, the accuracy of the CMOS temperature sensor structure mentioned above is about 0.1℃. Moreover, CMOS temperature sensor has a high power supply rejection ratio about -60dB and its work temperature range is usually between 0℃and 85℃. The power consumption is usually less than 1mW. But the lack of this kind of structure is over-dependence manufacturing matching. In fact, it is very difficult to fabricate two exactly same MOSFETs M1 and M2. If no matching, the performance of the circuit will decline and something unexpected will happen[4,5].

II. New Structure of CMOS Temperature Sensor

A high stable on-chip CMOS temperature sensor is proposed to solve the problem mentioned above. Fig. 2 shows the whole circuit diagram which include four parts that temperature sensor core circuit, operational amplifier, bias circuit and start circuit.

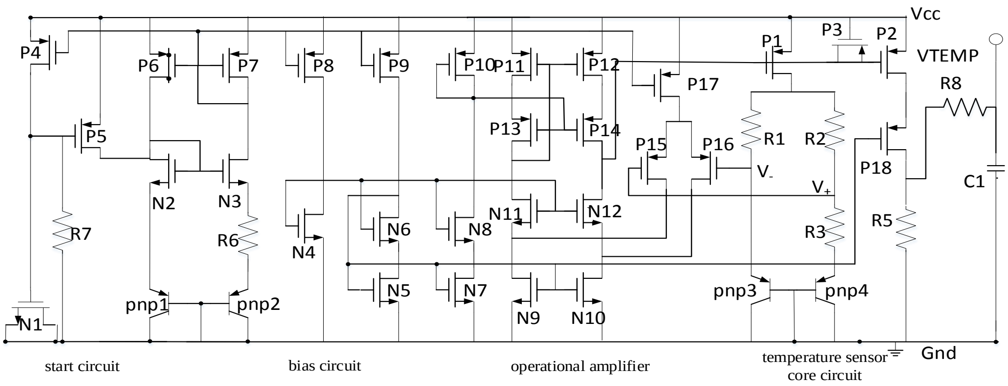

Figure 2 the circuit of CMOS temperature sensor

The circuit structure of fig. 1 need satisfy four-terminal balance in the same time. That is $V_+ = V_-$ and $I_2 = I_1$. In theory, it is impossible. As shown in the fig. 2, a P-type MOSFET P1 provides current for two branch and add R_1 and R_2 to make two branch current matching. Assuming that the current of P1 is I_{P1} and $V_+ = V_-$, the voltage between the two poles of the R_1 (U_{R1}) and R_2 (U_{R2}) are equal. When the value of R_1 and R_2 are same, the current of R_1 (I_{R1}) must be same as R_2 (I_{R1}). Under normal circumstances, the ratio of emitter junction area for pnp4 and pnp3 is 8. So the current of R_3 (I_{R3}) can be expressed, as shown in equation 3.

$$I_{R3} = \frac{V_{\text{bepnp3}} - V_{\text{bepnp4}}}{R_3} = \frac{\Delta V_{\text{be}}}{R_3} \qquad (3)$$

Where V_{bepnp3} and V_{bepnp4} is the base-emitter voltage of pnp3 and pnp4 and ΔV_{be} is the difference value of them. From the equation 2, I_{P1} and I_{P2} are proportional to temperature. When I_{P2} flows through R_5, a voltage (V_{TEMP}) will be generated and it is proportional to temperature.

Folded cascade amplifier is used in the structure shown in fig. 2 and the amplifier has a larger output impedance than diode amplifier. Due to the diode amplifier use common source as the output, the output impedance is low and it is difficult to make phase compensation without Miller compensation. However, Miller compensation must cause a problem that establish a way between input and output of the amplifier, which will make the PSRR of circuit reduce. The folded cascade amplifier do not exist the problem which exist in diode amplifier, so it is so easy to compensate the phase. Moreover, the folded cascade amplifier structure cannot cause oscillation because of the large output impedance. The function of bias circuit is generating some bias voltages for OP-AMP. As shown in the fig. 2, the gate voltage of P6 and P7 is very stable and the influence is small by the power fluctuation. And the gate voltage will be mirrored three times in the same time to provide bias voltage for OP-AMP. Unfortunately the bias circuit have two quiescent operating point but only one is needed, so a start circuit is necessary. The function of start circuit is to ensure the bias circuit working nonzero quiescent operating point. So far the inverter is usually used in the structure of start circuit, but the consumption is large. To reduce the consumption, a kind of start circuit is proposed shown as the fig. 2. When the system is powered on, P5 opens and then the bias circuit will start working. Meanwhile, P4 opens and the voltage of P5 will increase and this condition will continue until P5 shutdown. R_7 is a big resistance whose function is to help capacitor (N1) discharge. The start circuit end-of-job.

In the structure shown in fig. 2, two kinds of compensation is added. One is that a p-type MOSFET is added between the output of folded cascade amplifier and VCC, which can increase the phase margin of the amplifier without any other introducing interference. The other is that join the low pass filter at the output port, which can improve the PSRR in the high frequency. In general, the CMOS temperature sensor put forward in this paper is more stable than conventional CMOS temperature sensor.

III. Simulation Result

Four kinds of simulation has been done for the sensor including DC, AC, TRAN and STB. The relationship between the output voltages of temperature sensor and temperature is shown in fig. 3. It is obvious that the voltage is proportional to temperature highly. Fig. 4 is the slope of curve in figure 3 and it shows that the value of slope is limit between 2.605mV/℃ and 2.595mV/℃. By calculation, the maximal error is 0.33℃ in the whole temperature range.

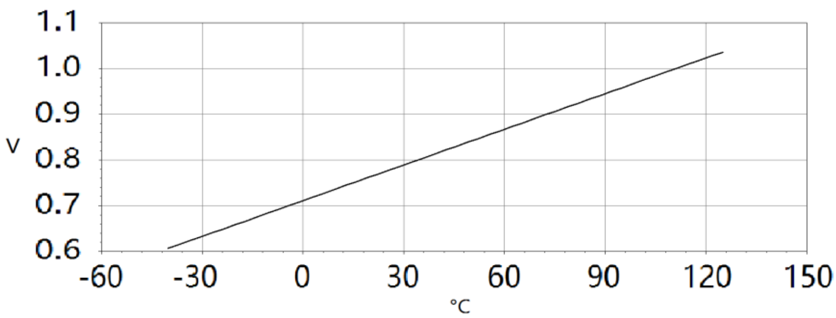

Fig. 3 the relationship between the output voltages of temperature sensor and temperature

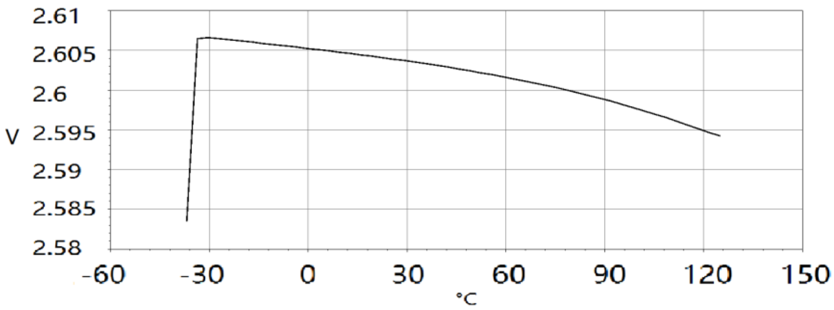

Fig. 4 slope of curve in Fig. 3

Fig. 5 is the transient simulation curve of the temperature sensor at 27℃. The figure shows that the built-up time is around 150us and the curve without over swing and long delay. Fig. 6 is the PSRR simulation curve of the temperature sensor. The value of PSRR is around -82dB in low frequency and -45dB@10kHz. To make the performance more vivid, a sine wave whose frequency is 10 kHz and amplitude is 180mV is added to the power supply and the simulation result is shown in fig. 7. The interference almost does not affect the output voltage of the sensor. So it is very stable.

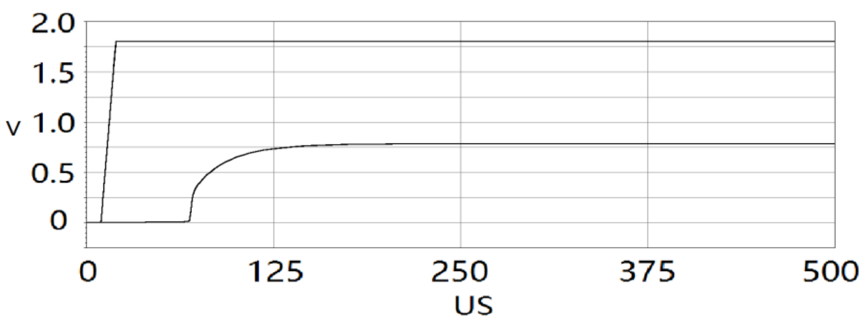

Fig. 5 the transient simulation curve of temperature sensor in 27℃

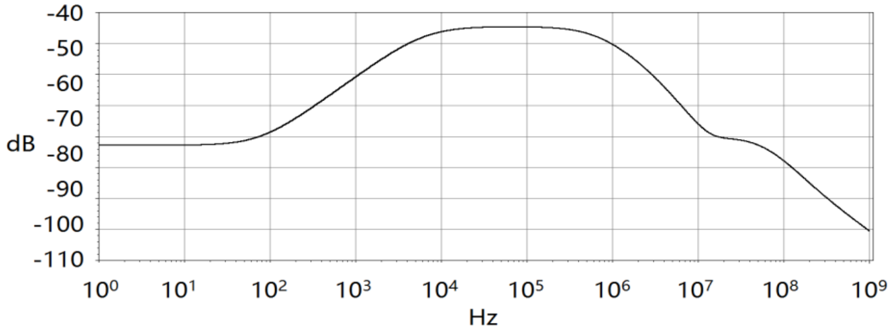

Fig. 6 the simulation result of PSRR of the temperature sensor

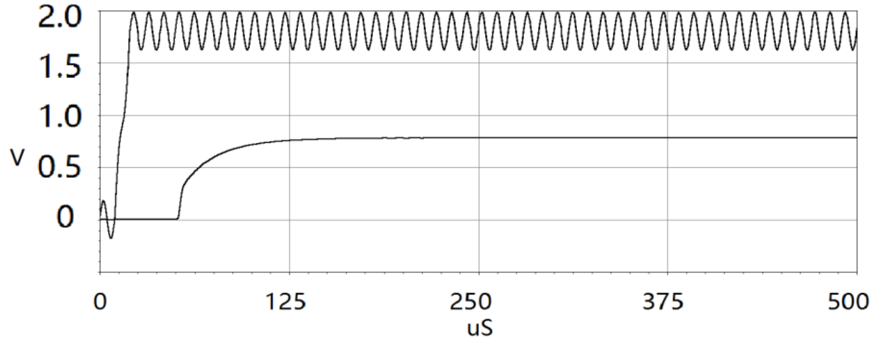

Fig. 7 the transient simulation curve with power interference

Figure 8 is the STB simulation curve of the sensor, in which the dotted line is the phase curve and the full line is the gain curve. From the fig. 8, the phase margin can be work out and its value is around 63º. It means that the sensor circuit is stable and no more built-up time.

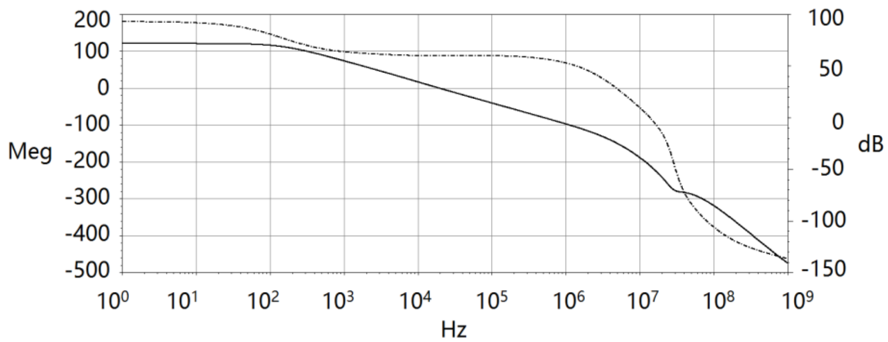

Fig. 8 the STB simulation curve of the sensor

IV. Conclusion

A high stable on-chip CMOS temperature sensor structure is presented. The sensor should work at 1.8V power supply and the working temperature range is between -40℃ and 125℃. The error is within ±0.02. The resolution of output voltage is 2.6mV/℃. The PSRR is -82dB@0Hz and -45dB@10kHz. The built-up time of voltage is less than 150us. The phase margin is about 63º. All simulation result can reflect that the sensor presented has a good working stable, which means it can be used many kinds of on-chip temperature measurement system.

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